**CECS 341 - Lab 4**

**“MIPS Write Back”**

**Due date: 03/05/19**

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I certify that this submission is my original work

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Lab Report: Lab Assignment 4 - “MIPS Write Back”

1. **Goal:** The goal of the lab is to perform the Write Back stage of the MIPS processor using a single MUX and a bunch of buses.
2. **Steps:**
   1. Step 1: Read over the entire instructions for the lab
   2. Step 2: Copy the code for the MUX
   3. Step 3: Copy the code for the test bench
   4. Step 4: Copy the skeleton code for the design file
   5. Step 5: Understand how the ALU and signals work for the Write Back instruction
   6. Step 6: Complete the skeleton code for the design file by filling in the correct inputs and outputs for the module
   7. Step 7: Check each answer with the solution provided and ensure the program is running correctly
3. **Results:** The results of this lab starts with outputting the test case number. After that, it will display the contents of the ALUoutw and the readdata registers. Then it will display whether the signals memtoreg, regwritem, and regwritew are turned on or not. The lab will also display resultw, which is the contents of the registers that writes back. The writeregm and writeregw carry the value of a particular register to be overwritten. For example, test case zero has ALUout has the output from the ALU operation which is 12153524 and readdata is the data that is read from memory. Memtoreg is set to zero so the ALUout is passed back into the register file. Since regwrite is one, the data will be written to a register. Finally, writereg is 04 because it is a value that selects a particular register to be overwritten.
4. **Conclusion:** I learned in this lab how to use the Write Back instruction in the ALU and how the signals work to control it. The challenge of this lab was understanding how the signals and registers were effected by the instruction.